Sub-10 nm EUV Lithography at 1000 W power

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In the past years, EUV lithography scanner systems have been widely adopted for manufacturing of state-of-the-art Integrated Circuits (IC), with critical dimensions down to 10 nm. With the upcoming introduction of a larger NA=0.55, these dimensions will even become smaller than 10 nm, and even higher NA systems are foreseen to potentially reach a critical dimension of 5 nm. This also tightens the requirements on CD and pattern placement control to ensure yielding devices.

At the same time, source powers have been continuously increasing to increase the productivity of the EUV scanners, and to keep up with increasing resist dose requirements for smaller features. The current ASML Source roadmap extends to 1000 W, and even higher powers are considered feasible.

This creates many novel challenges for the EUV scanner:

- Improved heating/cooling, since a large fraction of the higher source powers will be absorbed and converted to heat in the reticle, wafer and optics
- Improved plasma control, since plasma will increase with higher source powers
- Tighter particle control, also on backside of wafer and reticle
- Pellicles that can withstand power of up to 1000 W

This presentation will discuss these challenges and possible solution paths being explored.

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